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PTO/SB/05 (2/98)

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for nonprovisional applications under 37 CFR § 1.53(b))

Attorney Docket No.	850063.529C1
First Inventor or Application Identifier	Shin Hwa Li
Title	SEMICONDUCTOR STRUCTURE HAVING AN IMPROVED PRE-METAL DIELECTRIC STACK AND METHOD FOR FORMING THE SAME
Express Mail Label No.	EL615231713US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231**

1. [X] General Authorization Form & Fee Transmittal *(Submit an original and a duplicate for fee processing)*

2. [X] Specification [Total Pages] **10** *(preferred arrangement set forth below)*
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure

3. [X] Drawing(s) *(35 USC 113)* [Total Sheets] **2**

4. Oath or Declaration [Total Pages] **2**
   - a. [ ] Newly executed (original or copy)
   - b. [X] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)

5. [X] Incorporation By Reference *(useable if box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer-Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))

9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney

10. [ ] English Translation Document *(if applicable)*

11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations

12. [X] Preliminary Amendment

13. [X] Return Receipt Postcard

14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired

15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. [X] Other: Certificate of Express Mail
    Check

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information below and in a preliminary amendment*

[X] Continuation [ ] Divisional [ ] Continuation-In-Part (CIP) of prior Application No.: **09/061,667**

Prior application information: Examiner **Eaton, K** *Group / Art Unit* **2823**

[ ] Claims the benefit of Provisional Application No. _____

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Respectfully submitted,

TYPED or PRINTED NAME David V. Carlson REGISTRATION NO. 31,153

SIGNATURE _____ Date Aug 3, 2000

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Shin Hwa Li – Clendale, Arizona Annie Tissier – Scottsdale, Arizona
Filed	:	August 3, 2000
For	:	SEMICONDUCTOR STRUCTURE HAVING AN IMPROVED PRE-METAL DIELECTRIC STACK AND METHOD FOR FORMING THE SAME

Docket No.	:	850063.529
Date	:	August 3, 2000

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Assistant Commissioner for Patents:

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Respectfully submitted,

Seed Intellectual Property Law Group PLLC

Jeanette West/Susan Johnson

Enclosures:

Postcard
Check for $1560
Form PTO/SB/05
General Authorization Under 37 C.F.R. § 1.136(a)(3) and Fee Transmittal (+ copy)
Copy of Specification, Claims, Abstract (10 pages)
Copy of 2 Sheets of Drawings (Figures 1-6)
Copy of Declaration and Power of Attorney
Information Disclosure Statement, Form PTO-1449, and New Cited References (6)
Petition for 3-Month Extension of Time in Parent 09/061,667 (+ 2 Copies)

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EXPRESS MAIL NO. EL615231713US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Present Application:

Applicants	:	Shin Hwa Li and Annie Tissier
Title	:	A SEMICONDUCTOR STRUCTURE HAVING AN IMPROVED PRE-METAL DIELECTRIC STACK AND METHOD FOR FORMING THE SAME
Docket No.	:	98-P-009 (850063.529)
Date	:	August 3, 2000

Prior Application:

Examiner	:	Kurt Eaton
Art Unit	:	2823
Application No.	:	09/061,667

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents:

Please amend the above-identified application as follows:

In the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of pending United States Patent Application No. 09/061,667, filed April 16, 1998. --

In the Claims:

1. (Amended) A semiconductor structure, comprising:

a substrate;

a patterned [oxide] layer disposed over the substrate;

a layer of undoped silicate glass disposed over the patterned [oxide] layer;

a layer of borophosphorous silicate glass over the layer of undoped silicate glass;

a first planarized layer of plasma-enhanced tetraethyl orthosilicate over at least a portion of the layer of the borophosphorous silicate glass, and not overlaying at least a portion of the borophosphorous silicate glass layer; and

a second layer of plasma-enhanced tetraethyl orthosilicate overlaying the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with [at least a] the portion of the borophosphorous silicate glass [region] layer, not overlaid by the first layer of plasma-enhanced tetraethyl orthosilicate, the layers of the undoped silicate glass, borophosphorous silicate glass, planarized plasma-enhanced tetraethyl orthosilicate and second plasma-enhanced tetraethyl orthosilicate layer together forming a pre-metal dielectric stack.

4. (Amended) The structure of claim 3 wherein a combined thickness of the [oxide] patterned layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than approximately [15k] 15,000 angstroms.

6. (Amended) An integrated circuit, comprising:

a substrate;

a dielectric layer disposed on the substrate;

a layer of undoped silicate glass disposed on the dielectric layer;

an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass;

a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, the planar dielectric layer directly overlaying at least a portion of the borophosphorous silicate glass and leaving exposed so as to not directly overlay at least a portion of the borophosphorous silicate glass; and

a second dielectric layer disposed on the planar dielectric layer and the portions of the borophosphorous silicate glass which are not overlaid by the planar dielectric layer, the layers of undoped silicate glass, borophosphorous silicate glass, planar dielectric layer, and a second dielectric layer together composing a pre-metal dielectric stack.

REMARKS

This Preliminary Amendment, together with the continuation are filed in response to the Final Rejection mailed February 3, 2000. The Examiner objected to claims 1, 4 and 6 for various informalities in the language. In addition, the Examiner rejected claims 1, 3, 4, 9, 10 and 13 for matters relating to form under 35 U.S.C. § 112.

The claims have been amended to overcome the rejection as to matters of informalities and also the matters of form under 35 U.S.C. § 112, second paragraph. Accordingly, the claims should be allowable in this regard.

All claims were rejected over a combination of three prior art references, Kuo in view of applicants' admitted prior art, and further in view of Su et al. Applicants traverse this rejection and believe the claims are patentable in light of this combination of the prior art.

As the Examiner admits, and states, Kuo fails to show a first layer of PETEOS (in the claim, the full phrase is used of "plasma-enhanced tetraethyl orthosilicate"). On top of which is placed a second layer of PETEOS. Indeed, Kuo et al. do not teach or suggest two PETEOS layers, stacked one on top of the other. Neither, of course, is this feature found in applicants' own admitted prior art Figures 1-3. Kuo et al., as well as applicants' admitted prior art also failed to show the additional claimed feature of the first layer of PETEOS being a planarized layer which overlays at least a portion of a BPSG layer and leaves exposed at least some portion of this same BPSG layer so that the second layer of PETEOS overlays and is in direct contact with this BPSG layer. Since neither Kuo et al., nor applicants' admitted prior art planarize the first PETEOS layer by etching until exposing a portion of the BPSG layer, neither of these references can teach nor suggest this claimed feature. Further, neither of these references suggest a yet additional layer of PETEOS on top of the planarized first PETEOS layer which covers both the first PETEOS layer and the exposed portions of the BPSG layer. There are, therefore several

claimed features of claims 1 and 6 which are clearly not found in common or obvious from the two prior art references as combined. The Examiner attempts to rely on Su et al. to supply these missing teachings. Clearly, Su et al. is also deficient in a similar respect and does not supply the teachings which are missing from these two prior art references. First, Su et al. should be understood in the context that Figures 3A and 4A are of the same location, whereas Figures 3B and 4B are not of the same location on the chip and do not directly relate to or attempt to show the same features shown in Figures 3A and 4A. Figures 3B and 4B are not seen even relevant to the present invention since they do not show planarization and removal of material to expose a lower layer. Figures 3A and 4A show planarization of a layer 28 until polysilicon layer 23 is exposed. This polysilicon layer 23 is not a BPSG layer. Further, Su teaches deposition of a first dielectric 27 (a silicon oxide) followed by etching and removal of the dielectric. This is then followed by deposition of a second polysilicon layer which is patterned and etched. After this polysilicon layer is patterned and etched, another dielectric layer 28 is deposited, planarized, then on top of which a further oxide is positioned. This is not seen as relevant to applicants' present invention which has three dielectric layers positioned, one on top of the other before even a first etch is performed and then a fourth dielectric layer is positioned on top thereof. Further, there are no polysilicon layers or pattern and etching of electrical conductors in the middle of the applicants' invention. Su may be summarized as follows: Dielectric 27 formation plus poly 23 deposition plus etch plus dielectric 28 formation plus etch plus dielectric 30 formation. The numbers after each of the layers refer to those layers in Su. As can be seen, each step in Su et al. is followed by some type of etch. There is no example given of three dielectric layers positioned, one on top of the other without etch after which a planarization step takes place. This, indeed is what occurs with applicants' invention and creates the final structure as claimed in claim 1. In particular, applicants' invention can be contrasted with Su by seeing that the sequence of applicants' invention is as follows: Undope silicon glass (4) plus BPSG formation (6) plus PETEOS (38) plus planarization (cmp etch) plus second PETEOS (46). Su, therefore does not suggest the missing features from Kuo and applicants' admitted prior art. Indeed, he is expressly missing the layers as claimed in applicants' structure, and he certainly does not teach or suggest the missing feature of a second layer of PETEOS on top of and in contact with the BPSG layer

and also on top of and in contact with a first planarized PETEOS layer. These features are not found in nor are obvious from any combination of prior art.

The Examiner appears to make a rejection based completely on hindsight and without reference to any prior art in the remarks at the bottom of page 4, last full paragraph, and the top of page 5. The Examiner states that it would be obvious to one of ordinary skill in the art to remove PETEOS layer 22 to expose at least a portion of the BPSG layer which would then, according to the Examiner, obviously suggest an additional layer of PETEOS to be formed since removing portions of the first PETEOS layer would decrease the thickness of the premetal dielectric stack which would then decrease the aspect ratio of any subsequently formed contact opening. These suppositions by the Examiner are completely unwarranted and unsupported by the prior art. Clearly, no prior art shows these features. The Examiner seems to suggest that they would be obvious to one of ordinary skill in the art merely because it would be more desirable to make a more reliable device. However, no prior art is cited to support the Examiner's proposition of these particular layers. If the Examiner is going to maintain this rejection and the reasoning for the obviousness-type statement, reference to a particular piece of prior art is respectfully requested.

It is believe that these features are in fact not at all obvious. Applicants disagree that it would be obvious to one of ordinary skill in the art to perform the etching of the first layer of PETEOS until it exposes a portion of the BPSG layer. Nor would it be obvious to add the additional PETEOS layer which is in contact with both the first PETEOS layer and the BPSG layer. No prior art shows or even suggests as obvious the features stated by the Examiner as being obvious. Again, applicants disagree that such features would be obvious and believe that they are both novel and not obvious to any of skill in the art.

For example, the Examiner also cited in this Office Action a reference from Murao, U.S. Patent No. 5,518,962. As can be seen, he deposits two PETEOS layers, 130A and 131. However, he does not planarize the first PETEOS layer 130A until it exposes the BPSG layer 120. Thus, Murao teaches directly away from and the opposite of applicants' present invention by failing to planarize and etch the first layer 130A until it exposes the BPSG layer 120. Other prior art documents are equally deficient in this regard. Thus, applicants can only conclude that it would not be obvious to one of skill in the art, and there is no prior art with

which Kuo, Su et al., or even its own admitted prior art can be combined to render these features obvious.

In the second half of paragraph 14, on page 5, the Examiner notes that the specification contains no disclosure to the critical nature of the claimed features regarding the extent of etching to achieve planarization of the PETEOS layer. He concludes in the paragraphs that applicants must show that the chosen alternative elements are critical. Applicants strongly disagree. It is not a requirement of U.S. patent law, nor would it be expected that the specification of such semiconductor process technology contain statements regarding whether certain steps are of a critical nature. Such showing of "critical nature" is not a requirement for patentability. The present claimed structure is novel. The present claimed structure is not obvious in light of the prior art. There is no need for Applicants to provide statements in their own specification regarding the critical nature of any particular steps, nor is it desirable to do so in U.S. patent specifications. All that is required is that disclosure of the claimed invention be in a manner that would enable it to be manufactured, that it be in the inventor's best mode, and that it be novel and not obvious in light of the prior art. These are all met by applicants' disclosure and claims. Allowance of the claims is respectfully requested.

Applicants' U.S. attorney recently received the European search report. The European search report was issued June 19, 2000, and received by applicants' U.S. counsel on July 27, 2000, approximately a month later. Applicants are therefore submitting the European search report together with all art cited therein in an idea as attached herewith. Since applicants were not aware of the prior art until within the last few days, the fee for filing late prior art is not needed.

Applicants' attorney has reviewed the prior art from the European search report and does not see any prior art which is any more relevant than what the Examiner has found in the current U.S. search report. For example, applicants note that much of it is either not as relevant, or merely cumulative. The European search report contains, for example, the European version of the Murao patent previously cited by this Examiner. It contains other documents which are also not seen as any more relevant than those documents already considered by the U.S. Examiner.

Since the claims are clear and allowable over all prior art of record, allowance of all claims is respectfully requested.

Respectfully submitted,

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A SEMICONDUCTOR STRUCTURE HAVING AN IMPROVED PRE-METAL DIELECTRIC STACK AND METHOD FOR FORMING THE SAME

TECHNICAL FIELD

The invention relates generally to a semiconductor structure that includes an improved pre-metal dielectric (PMD) stack, and more specifically to a structure that includes an undoped silicate glass/borophosphorous silicate glass/plasma-enhanced tetraethyl orthosilicate (USG/BPSG/PETEOS) PMD stack and a method for forming the same.

BACKGROUND OF THE INVENTION

Semiconductor processes for manufacturing integrated circuits often require forming a protective layer, or layers, to, *e.g.*, reduce contamination by mobile ions, prevent unwanted dopant diffusion between different layers, and isolate elements of an integrated circuit. Typically, such a protective layer is formed with silicon-based dielectrics, such as silicon dioxide, which may take the form of undoped silicate glass (USG), borosilicate glass (BSG), or borophosphorous silicate glass (BPSG). BSG is typically formed by doping USG with Boron. Likewise, BPSG is typically formed by doping USG with both Boron and Phosphorous. If these dielectrics are disposed beneath the first metal layer of the integrated circuit, they are often referred to as pre-metal dielectrics (PMD).

A conventional PMD stack often includes a USG layer disposed on a semiconductor substrate, and a BPSG layer disposed on the USG layer. Typically, a BPSG film layer has a number of advantages over a USG layer. For example, a BPSG layer is often a better moisture barrier than a USG layer. Also, the phosphorous ions in a BPSG layer trap mobile sodium (Na) or other ions. This phenomenon is called "gettering," and it is sometimes used to reduce or eliminate an unwanted shift in a transistor's threshold voltage V_T caused by mobile ions trapped in the gate oxide of the transistor. Additionally, the Boron ions decrease the viscous flow temperature of the BPSG layer. This facilitates reflow of the BPSG layer, and thus improves the reflow

planarization of the BPSG layer surface and allows for the filling of gaps with fewer voids. A downside of BPSG is that Boron and Phosphorous ions may diffuse from the BPSG into an underlying silicon region such as a silicon substrate. Such diffusion may cause undesirable changes in the doping profile of the silicon region. Therefore, to prevent such diffusion, the PMD stack includes a USG layer beneath the BPSG layer. The USG layer acts as a barrier to such diffusion.

Figure 1 is a cross-section of a portion of a conventional semiconductor structure 1. The structure 1 has a patterned field-oxide layer 2 that defines active regions 8 in a semiconductor substrate 10. In one embodiment, the field oxide 2 has a thickness between approximately 3k to 6k angstroms. A gate structure 12 is disposed over the active region 8, and a layer 14 is disposed over a segment of the field oxide 2. A USG layer 4 having a thickness between approximately 1k - 2k angstroms is conventionally formed over the surface of the structure 1. A relatively thick BPSG layer 6 having a thickness between approximately 12k - 25k angstroms is subsequently formed over the USG layer 4. In one embodiment, the thickness of the BPSG layer 6 is at about 18k angstroms.

Referring to Figure 2, after the BPSG layer 6 has been formed, the structure 1 is planarized using a conventional chemical mechanical polishing (CMP) process. The CMP process reduces the combined thickness of all layers above the substrate 10, *i.e.*, from the bottom of the field oxide 2 all the way to the top of the BPSG layer 6, to a value yk. In one embodiment, yk is approximately 12k angstroms. The layer 4 and the polished layer 6 form a PMD stack 17.

Referring to Figure 3, an optional plasma-enhanced tetraethyl orthosilicate (PE-TEOS) redeposition dielectric layer 16 having a thickness between approximately 2k - 4k angstroms may be conventionally formed over the polished BPSG layer 6. Therefore, when present, the layer 16 composes part of the PMD stack 17.

As the semiconductor industry increasingly relies on the CMP technique for planarization in today's high-density integrated circuits, drawbacks of the USG/BPSG PMD stack in connection with the CMP technique become more

prominent. First, Boron and Phosphorous dopants in the BPSG layer 6 often are not uniformly distributed across and against the depth of the semiconductor wafer. This non-uniform distribution of the boron and/or phosphorous dopants often causes uneven thickness of the BPSG layer 6 even after CMP. Second, forming the BPSG layer 6, which is typically accomplished by a atmospheric pressure chemical vapor deposition (APCVD) process, is often a low-throughput and high maintenance process. As a result, using a relatively thick sacrificial BPSG layer 6 for the PMD 17 is often burdensome for manufacturing today's high-density integrated circuits. Additionally, the BPSG layer 6 often is too soft for a CMP process to adequately smoothen or planarize the surface of the layer 6.

SUMMARY OF THE INVENTION

In one embodiment of the invention, a semiconductor structure includes a substrate, a dielectric layer disposed over the substrate, an undoped silicate glass layer disposed over the insulator layer, a borophosphorous silicate glass layer disposed over the undoped silicate glass layer, and a planar dielectric layer disposed over the borophosphorous silicate glass, the undoped silicate glass layer, the borophosphorous silicate glass layer, and the planar dielectric layer together forming a pre-metal dielectric stack layer. In one embodiment, the planar dielectric layer includes plasma-enhanced tetraethyl orthosilicate.

BRIEF DESCRIPTION OF THE DRAWING

Figure 1 is a cross-section of a conventional semiconductor structure.

Figure 2 shows the semiconductor structure of Figure 1 after it has been subjected to a CMP process.

Figure 3 shows the semiconductor structure of Figure 2 after the formation of an optional PE-TEOS redeposition layer.

Figure 4 is a cross-section of a semiconductor structure formed according to an embodiment of the invention.

Figure 5 shows the semiconductor structure of Figure 4 after it has been subjected to a CMP process.

Figure 6 shows the semiconductor structure of Figure 5 after the formation of an optional PE-TEOS redeposition layer over the polished USG/BPSG/PE-TEOS stack.

DETAILED DESCRIPTION OF THE INVENTION

Figures 4-6 shows a process for forming a PMD stack 20 according to one embodiment of the invention. Like reference numerals are used to reference elements in common with Figures 1-3.

Referring to Figure 4, a layer 38 is formed over the BPSG layer 6 before CMP. In one embodiment, the layer 38 is conventionally formed from plasma-enhanced tetraethyl orthosilicate (PE-TEOS). The layer 38 acts as a sacrificial layer for the CMP process. In one embodiment, the thickness of the layer 38 is between approximately 8k - 20k angstrom, for example about 12k angstroms. The thickness of the BPSG layer 6 is between approximately 1.5k - 8k angstroms, for example 6k angstroms. The thickness of the USG layer 4 is between approximately 1k - 3k angstroms, and the thickness of the field oxide 2 is between approximately 3k - 6k angstroms.

Referring to Figure 5, after the layer 38 is formed, the structure 1 then goes through the CMP process. In one embodiment, the layer 38 is polished until the BPSG layer 6 is exposed. In another embodiment, the polishing stops before the BPSG layer 38 is exposed. In yet another embodiment, the polishing endpoint is empirically determined using a test wafer (not shown). Alternatively, endpoint data provided by the manufacturer of the CMP equipment may be used. After the CMP, the combined thickness yk of all layers, *i.e.*, measured from the bottom of the field oxide 2 to the top of the layer 38, is between approximately 8k to 15k angstroms. In one embodiment, yk is approximately 13k angstroms. Thus, the layers 4 and 6 and the polished layer 38 together compose the PMD stack 20.

Referring to Figure 6, subsequent to the CMP, an optional redeposition layer 46 may be formed on the layer 38. In one embodiment, the layer 46 is formed from PE-TEOS, has a thickness of approximately 2k angstroms, and composes part of the PMD 20. In another embodiment, the layer 46 is formed from TEOS.

All subsequent process steps, such as, *e.g.*, opening windows for tungsten plugs and metallization and finishing manufacturing of the semiconductor structure 1, are conventional and are thus not discussed in detail.

In embodiments where the layer 38 is formed from PE-TEOS, the layer 38 is often harder than the BPSG layer 6, and thus allows the PMD stack 20 to maintain the advantages of the conventional USG/BPSG stack while eliminating the disadvantages of polishing the BPSG layer 6. Furthermore, PE-TEOS has a higher throughput rate during processing than BPSG. Therefore, when formed from PE-TEOS, the layer 38 aids in reducing the processing time by allowing the BPSG layer 6 to have a reduced thickness. Because the thickness of the BPSG layer 6 is reduced, the layer 6 processing time is significantly reduced.

Specifically, in embodiments where the layer 38 is formed from PE-TEOS, the process for PE-TEOS deposition is up to about twice the throughput rate as compared with that of the BPSG deposition process. Furthermore, the PE-TEOS layer 38 is often deposited by using the plasma-enhanced chemical vapor deposition (PECVD) process. Thus, unlike the BPSG process which often requires substantial efforts of equipment cleaning after deposition to avoid defects, equipment for PE-TEOS deposition often require less efforts to clean after deposition. This will cause less down time for the PE-TEOS deposition process than for the BPSG deposition process. In addition, the CMP process normally polishes the PE-TEOS layer 38 more uniformly than it would polish the BPSG layer 6 since there is no problem of non-uniform distribution of boron and phosphorous ions in the PE-TEOS layer 38. Another advantage of the present invention is that the same PE-TEOS deposition recipe can be used in the CMP process for both the PMD stack 20 and later inter-level dielectric (ILD) layers (not shown), which are dielectric layers conventionally formed after first

metallization of the semiconductor structure 1. This often simplifies the manufacturing process of the semiconductor structure 1.

Although the detailed description discloses various embodiments of the invention, other embodiments may be made without deviating form the scope of the invention. In particular, the layer 38 may be formed using a High-Density Plasma Chemical Vapor Deposition (HDPCVD or HDP) technique or even a traditional CVD technique. In alternative embodiments, the respective thicknesses of the layer 38, the USG and BPSG layers 4 and 6, and the field oxide 2 can be fine-tuned to obtain optimal desired characteristics, *e.g.*, gettering effect of mobile ions or to improve the yield of the manufacturing process.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

What is claimed is:

1. A semiconductor structure, comprising:

a substrate;

a patterned oxide layer disposed over the substrate;

a layer of undoped silicate glass disposed over the patterned oxide layer;

a layer of borophosphorous silicate glass over the layer of undoped silicate glass; and

a layer of plasma-enhanced tetraethyl orthosilicate over the layer of borophosphorous silicate glass, the layers of undoped silicate glass, borophosphorous silicate glass, and plasma-enhanced tetraethyl orthosilicate together forming a pre-metal dielectric stack.

2. The structure of claim 1 wherein the layer of borophosphorous silicate glass has a thickness between approximately 2k and 8k angstroms.

3. The structure of claim 1 wherein the layer of plasma-enhanced tetraethyl orthosilicate is planar.

4. The structure of claim 3 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the layer of plasma-enhanced tetraethyl orthosilicate is less than approximately 15k angstroms.

5. The structure of claim 3, further comprising a layer of tetraethyl orthosilicate disposed over the layer of plasma-enhanced tetraethyl orthosilicate.

6. An integrated circuit, comprising:

a substrate;

a dielectric layer disposed on the substrate;

a layer of undoped silicate glass disposed on the dielectric layer;

an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass; and

a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, the layers of undoped silicate glass, borophosphorous silicate glass, and planar dielectric together composing a pre-metal dielectric stack.

7. The integrated circuit of claim 6 wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

8. The integrated circuit of claim 6, further comprising a dielectric layer disposed on the planar dielectric layer.

9. The integrated circuit of claim 6, further comprising:

a layer of tetraethyl orthosilicate disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

10. The integrated circuit of claim 6, further comprising:

a layer of plasma-enhanced tetraethyl orthosilicate disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

11. A method for forming a semiconductor structure, the method comprising:

forming a patterned oxide layer over a substrate;

forming a USG layer on the patterned oxide layer and exposed portions of the substrate;

forming a BPSG layer on the USG layer;

forming a PE-TEOS layer over the BPSG layer; and

planarizing the PE-TEOS layer to form a pre-metal dielectric stack.

12. The method of claim 11 wherein the planarizing is accomplished by a chemical-mechanical polishing technique.

13. The method of claim 11, further comprising forming a TEOS layer on the planarized PE-TEOS layer.

14. The method of claim 11 wherein the BPSG layer is between approximately 2k to 8k angstroms thick.

15. The method of claim 11 wherein the USG layer is between approximately 1k to 4k angstroms thick.

16. The method of claim 11 wherein a total thickness of the oxide layer, the USG layer, the BPSG layer, and the planarized PE-TEOS layer is less than approximately 15k angstroms.

17. The method of claim 13 wherein the TEOS layer is between approximately 1k to 5k angstroms thick.

18. The method of claim 11, further comprising forming a PE-TEOS layer on the planarized PE-TEOS layer.

19. The method of claim 18 wherein the PE-TEOS layer is between approximately 1k to 5k angstroms thick.

A SEMICONDUCTOR STRUCTURE HAVING AN IMPROVED PRE-METAL DIELECTRIC STACK AND METHOD FOR FORMING THE SAME

ABSTRACT OF THE DISCLOSURE

A semiconductor structure includes a substrate, a dielectric layer disposed on the substrate, a layer of undoped silicate glass disposed on the dielectric layer, a layer of borophosphorous silicate glass on the layer of undoped silicate glass, and a planar dielectric layer disposed on the layer of borophosphorous silicate glass, the layers of undoped silicate glass, borophosphorous silicate glass, and planar dielectric together forming a pre-metal dielectric stack. The planar dielectric may include plasma-enhanced tetraethyl orthosilicate.

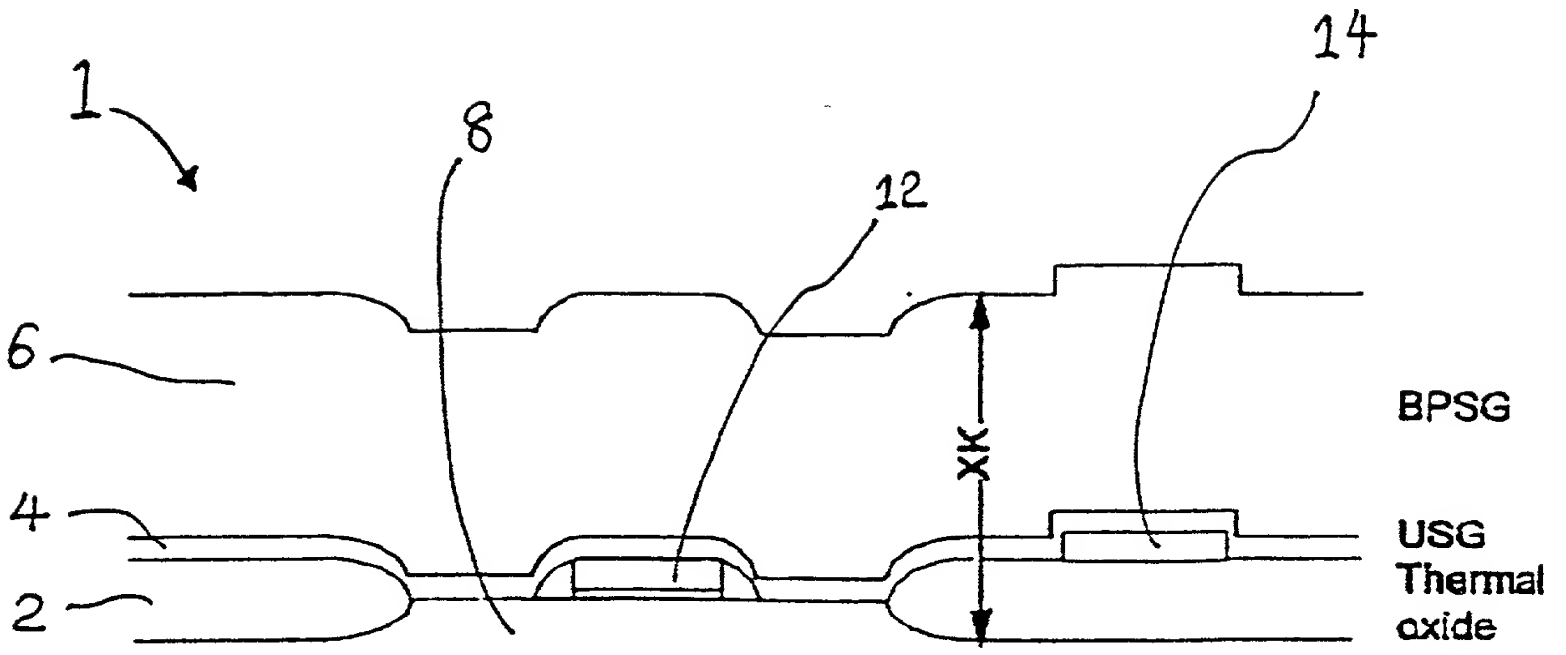


Figure 1 (Prior Art)

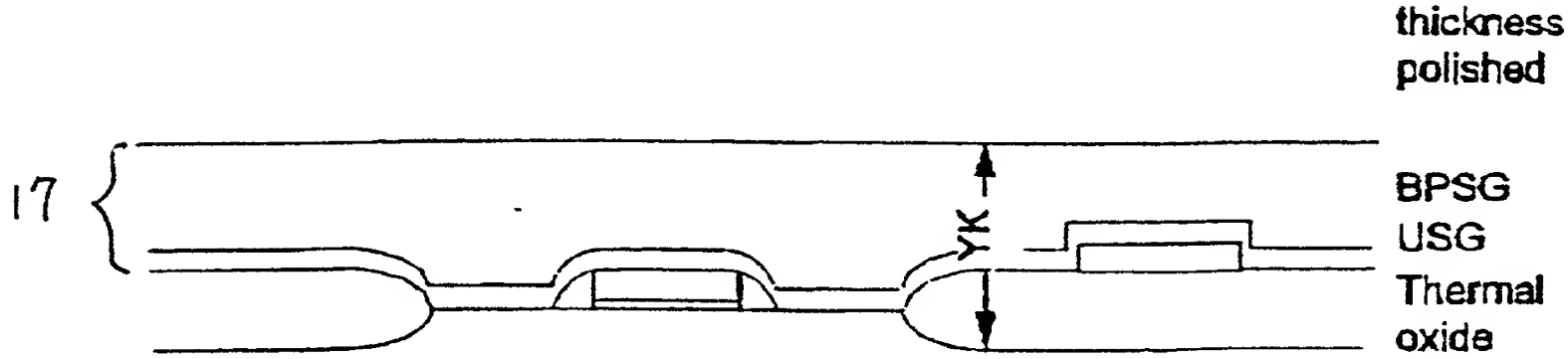


Figure 2 (Prior Art)

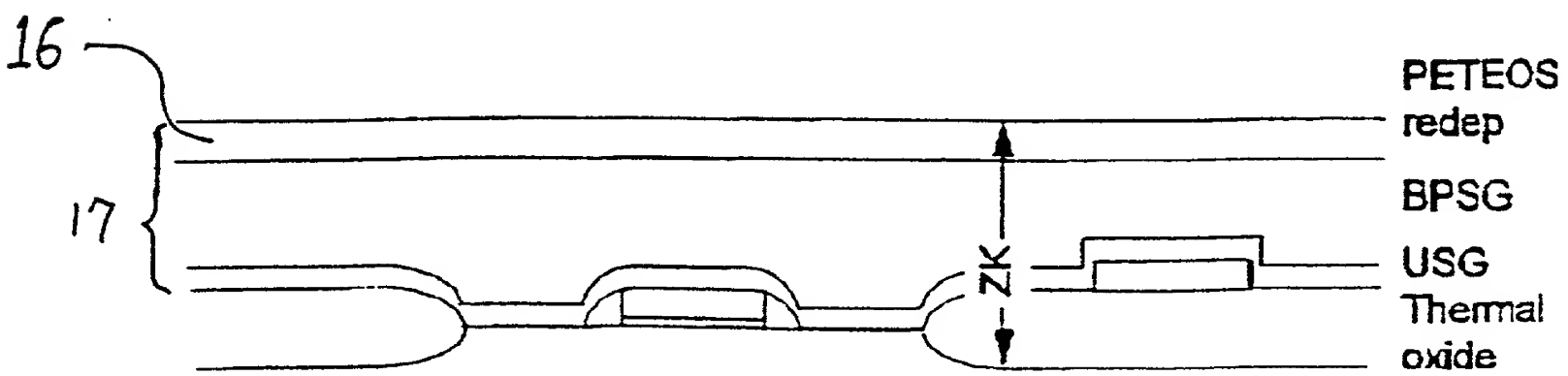
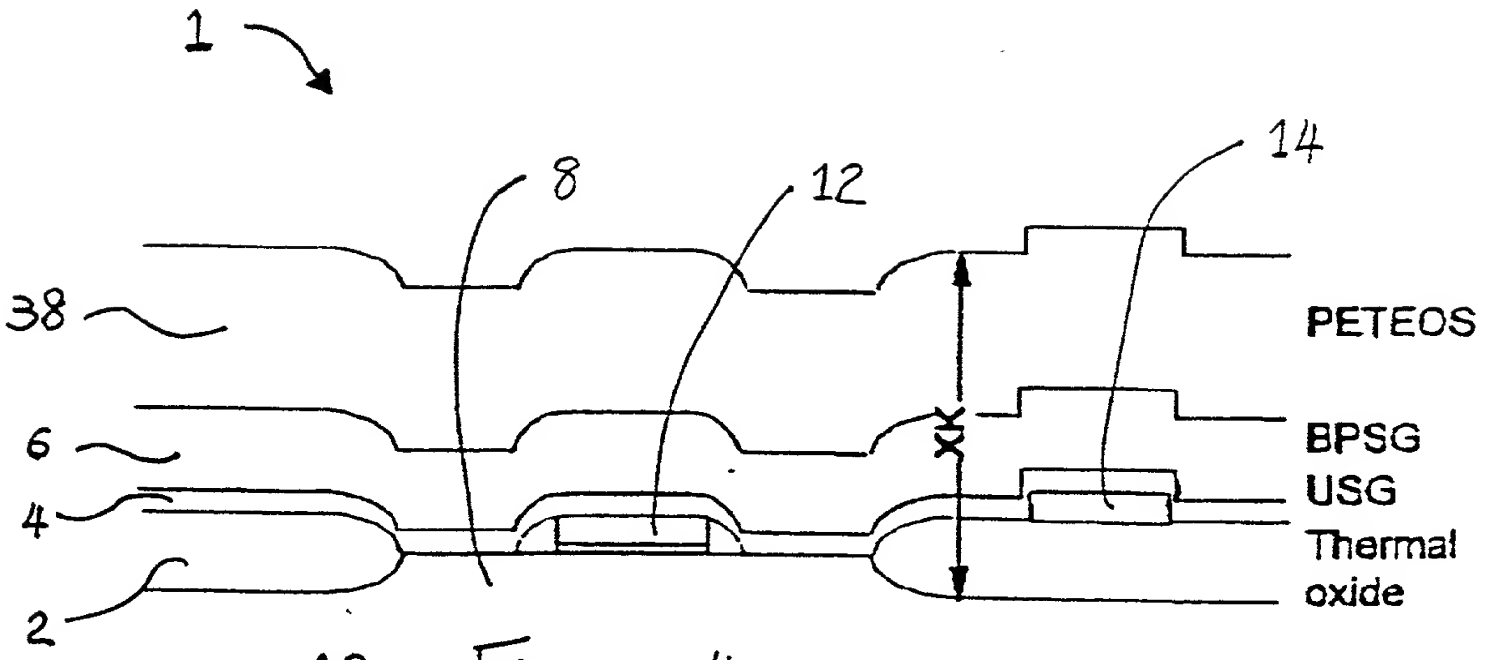


Figure 3 (Prior Art)



10 Figure 4

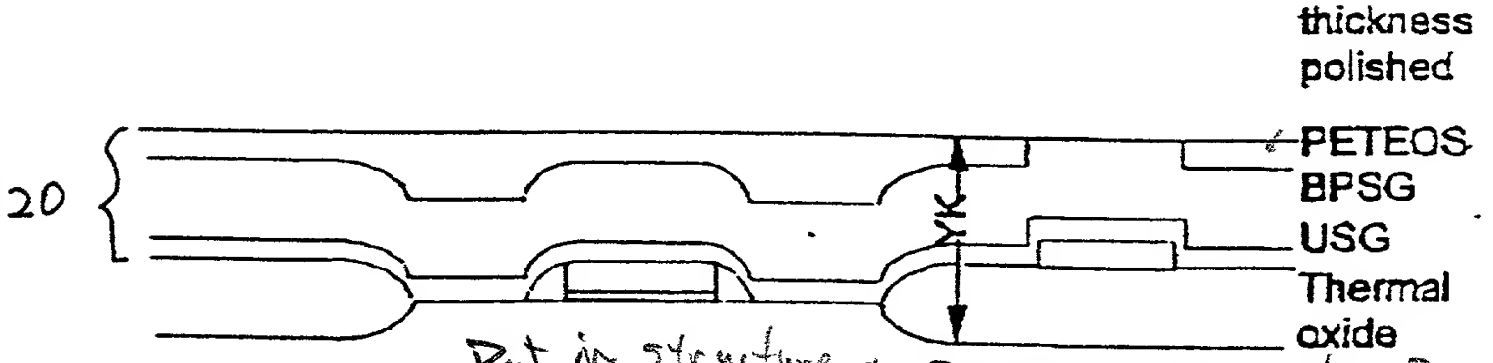


Figure 5

Put in structure claims The PTEOS overlayer the Planarized PETOES caned Directly overlayer on contacting the BPSG layer

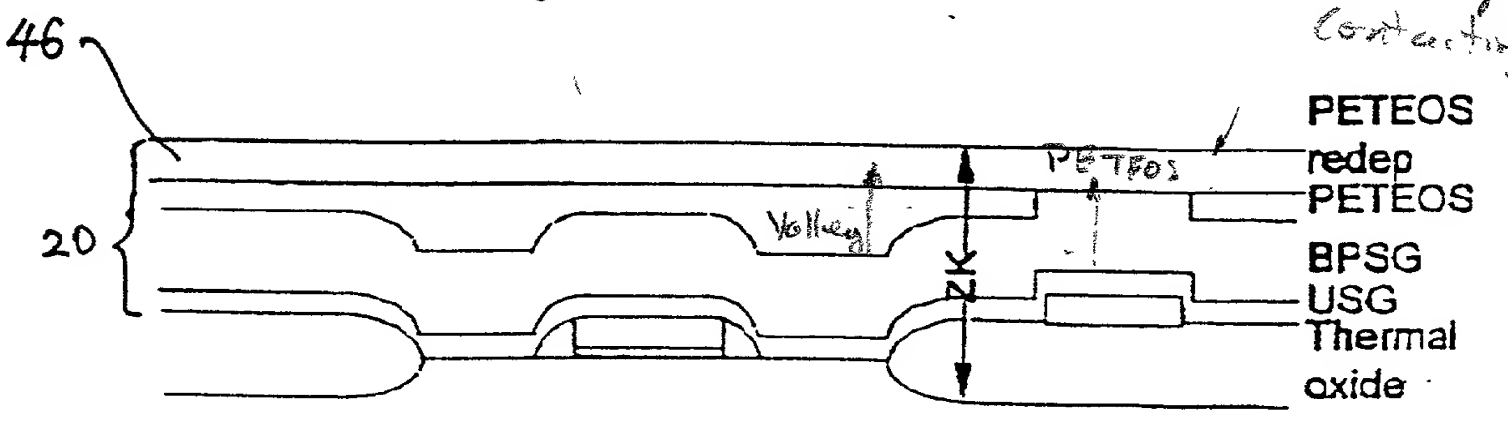


Figure 6

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Docket No. 850063.529

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As the below-named inventors, we hereby declare that:

Our residences, post office address, and citizenship are as stated below under our names.

We believe that we are the original inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled

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which is described and claimed in the foregoing specification and for which a patent is sought.

We hereby state that we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to herein (if any).

We acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

POWER OF ATTORNEY: As the named inventors, we hereby appoint the following attorneys and agent with full power of substitution and revocation to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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